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APPLICATION NUMBER: *60/544,702*
FILING DATE: *February 12, 2004*
RELATED PCT APPLICATION NUMBER: *PCT/US04/44097*

Certified by

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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No. EL 753209174 US

INVENTOR(S)		
Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
David	Okada	Chandler, AZ

Additional inventors are being named on the _____ *separately numbered sheets attached hereto*

TITLE OF THE INVENTION (500 characters max)

METAL SYSTEM FOR DIRECT DIE ATTACHMENT

Direct all correspondence to: **CORRESPONDENCE ADDRESS**

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City		State		Zip	
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ENCLOSED APPLICATION PARTS *(check all that apply)*

☑ Specification *Number of Pages* 6 ☐ CD(s), Number _____

☑ Drawing(s) *Number of Sheets* 4 ☐ Other (specify) _____

☐ Application Date Sheet. See 37 CFR 1.76

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

☑ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check or money order is enclosed to cover the filing fees.

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FILING FEE Amount ($): $80.00

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☑ No.

☐ Yes, the name of the U.S. Government agency and the Government contract number are: _____

Respectfully submitted,

SIGNATURE William C. Hwang

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Date February 12, 2004

REGISTRATION NO. 36,169 *(if appropriate)*

Docket Number: 104023-679-PRO

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

This collection of information is required by 37 CFR 1.51. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Provisional Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Country:	US
Application No.:	TBA
Filing Date:	February 12, 2004
Inventors:	David Okada
Title:	METAL SYSTEM FOR DIRECT DIE ATTACHMENT
Atty Docket No.:	104023-679-PRO

CERTIFICATE OF "EXPRESS MAILING"

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Submitted herewith are the following items:

1. Provisional Application For Patent Cover Sheet (in duplicate) (2 pages);
2. Provisional Application of David Okada (10 pages);
3. This Certificate of Express Mailing bearing Express Mailing Label No. and deposit date stated above (1 page); and
4. Return Receipt Postcard.

TOTAL PAGES IN THIS SUBMISSION: 13 + postcard

Francene Sawyer

Francene Sawyer

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Francene Sawyer February 12, 2004

Francene Sawyer Date

U.S. Provisional Patent Application Entitled

METAL SYSTEM FOR DIRECT DIE ATTACHMENT

Inventor:

David Okada, 5681 W Park Ave., Chandler, AZ 85226

TITLE

[0001] METAL SYSTEM FOR DIRECT DIE ATTACHMENT

FIELD OF THE INVENTION

[0002] This invention generally relates to a system for mounting semiconductor dies on a circuit board.

BACKGROUND OF THE INVENTION

[0003] A typical surface mountable semiconductor components consists of a semiconductor die attached to a lead frame, wire bonded, and encapsulated into a plastic package with exposed leads. Soldering the leads to the printed circuit board provides mechanical, thermal, and electrical connections to the semiconductor die.

[0004] Figure 1 shows a typical wire bonded die. Wire bonds add parasitic inductance and series resistance to the electronic component/circuit. The added inductance and resistance is undesirable for many devices, including high frequency devices, high speed devices, and low on-resistance power semiconductor devices. The lead frame provides the primary thermal conduction path for the die. The length of the thermal path to the printed circuit board and lead frame design and composition limits the thermal performance of a package.

[0005] Wire bonds and lead frames can be eliminated using flip chip wafer bumping packaging. Examples of two available flip chip processes are shown in Figure 2. Additional processing is performed to the top surface of the semiconductor die 210 to attach a solder ball 220 or build a raised conductive region which may be made of silicon or a metallic material such as copper, nickel or other metal or alloy, with a top coating of solder. The processing creates a conductive region 260 that allows solder ball 220 or

another conductive region to electrically contact silicon die 210. This allows the device to be attached to the printed circuit board. A disadvantage of the solder ball approach is the limited contact area of the ball to the die surface and printed circuit board. This reduces both the thermal and electrical conduction areas increasing both the thermal and electrical resistance. The thermal and electrical paths are long, approximately the diameter of the solder ball. The limited contact area of the ball also results in the limited mechanical strength of the bond between the die and printed circuit board.

[0006] The copper pedestal bump using pillar 230 is an improvement over the solder ball. Current and heat flows through copper which is significantly more thermally and electrically conductive than solder. The standard height of pillar 230 (approx. 100um) adds to both the thermal and electrical resistance. Both bumping processes involve multiple processing steps and require specialized equipment which adds cost.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The figures below depict various aspects and features of the present invention in accordance with the teachings herein.

DESCRIPTION OF THE INVENTION

[0008] The aspects, features and advantages of the present invention will become better understood with regard to the following description with reference to the accompanying drawings. What follows are preferred embodiments of the present invention. It should be apparent to those skilled in the art that the foregoing is illustrative only and not limiting, having been presented by way of example only. All the features disclosed in this description may be replaced by alternative features serving the same purpose, and equivalents or similar purpose, unless expressly stated otherwise. Therefore,

numerous other embodiments of the modifications thereof are contemplated as falling within the scope of the present invention as defined herein and equivalents thereto. Use of absolute terms, such as "will not," "will," "shall," "shall not," "must," and "must not," are not meant to limit the present invention as the embodiments disclosed herein are merely exemplary.

[0009] The present invention is applicable to all types of semiconductor die, such as integrated circuits, discrete semiconductor devices, sensors, micro-machined structures, etc. -- one aspect of the present invention disclosed here is shown in Figure 3.

[0010] In particular, solderable metal contact regions 310 are formed directly onto the top metal surface 320 of die 300. The solderable metal regions 310 allows die 300 to be directly soldered onto a printed circuit board. Advantages of this system is that it requires only the deposition and patterning of thin metal film layers on the order of 1um thick onto solderable metal regions 310. Examples of solderable films are TiCu, TiNiAg, or AlNiVCu. These films can be used alone or covered with a top layer of solder. The solder layer will help to prevent oxidation of the exposed metal and may simplify mounting to the printed circuit board.

[0011] An illustration of a die mounted onto the printed circuit board is shown in Figure 4. In particular, the die with a solderable metal system can be mounted to the printed circuit board 430 using conventional surface mount techniques. A thin layer of solder paste 410 can be deposited with a stencil onto the printed circuit board 430. The die 300 is then placed into the proper location and lowered until it is in contact with paste 410. The printed circuit board 430 assembly is then heated to approximately 200C until the solder reflows. The solderable metal patterns on the die are then directly soldered to

the copper printed circuit board traces 420 thereby forming a mechanical, electrical, and thermal connection.

[0012] If the optional solder layer is added to the solderable metal system, it is not necessary to apply the solder paste 410. The solder on the die, once reflowed, will be sufficient to attach the die to the printed circuit board, further simplifying the assembly process.

[0013] Advantages of this invention are summarized as follows:

- Simplicity of the packaging
- Ease of manufacturing
- Simplicity of mounting device to the printed circuit board
- Enhanced thermal performance of the package.
- Very short thermal path from the semiconductor die to the printed circuit board.
- Contact areas can be maximized to increase area of thermal path
- thereby reducing the thermal resistance
- Very low electrical resistance from die surface to the printed circuit board.
- Short current path from die to printed circuit board.
- Contact areas can be increase to further minimize the series resistance.
- No wire bond or lead frame inductance and resistance.

CONCLUSION

[0014] Having now described preferred embodiments of the invention, it should be apparent to those skilled in the art that the foregoing is illustrative only and not limiting, having been presented by way of example only. All the features disclosed in

this specification (including any accompanying claims, abstract, and drawings) may be replaced by alternative features serving the same purpose, and equivalents or similar purpose, unless expressly stated otherwise. Therefore, numerous other embodiments of the modifications thereof are contemplated as falling within the scope of the present invention as defined by the appended claims and equivalents thereto.

Semiconductor Die with Solderable Metal System Allowing Direct Surface Mounting to Printed Circuit Boards

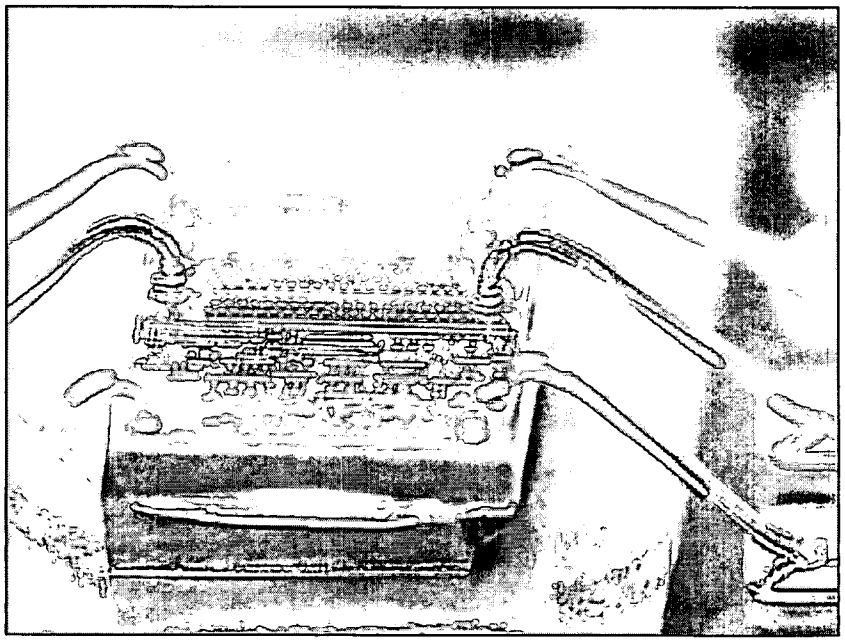


Figure 1. Example of Wire Bonding Used to Form the Electrical Connections to the Semiconductor Die

Semiconductor Die with Solderable Metal System Allowing Direct Surface Mounting to Printed Circuit Boards

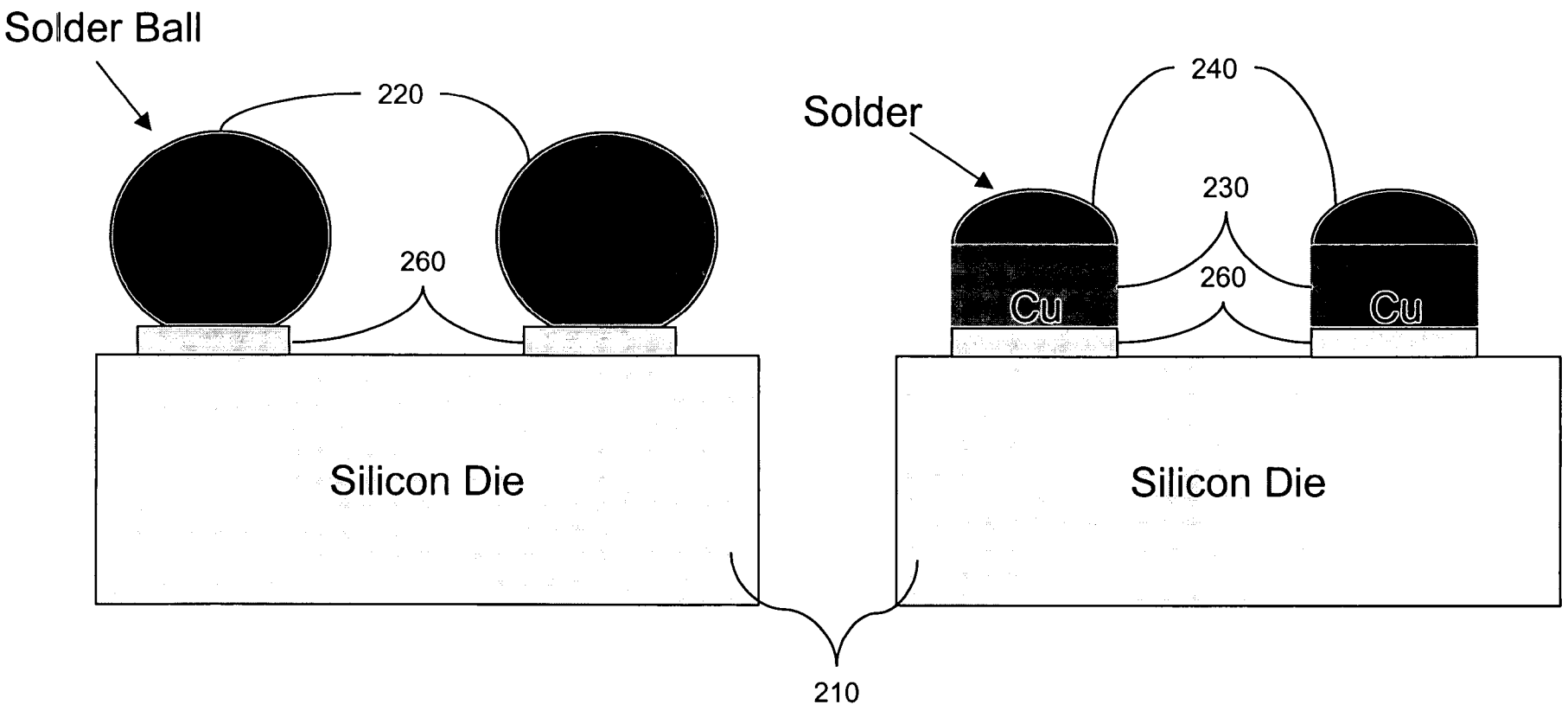


Figure 2. Typical Flip Chip Wafer Bumping Packages

Semiconductor Die with Solderable Metal System Allowing Direct Surface Mounting to Printed Circuit Boards

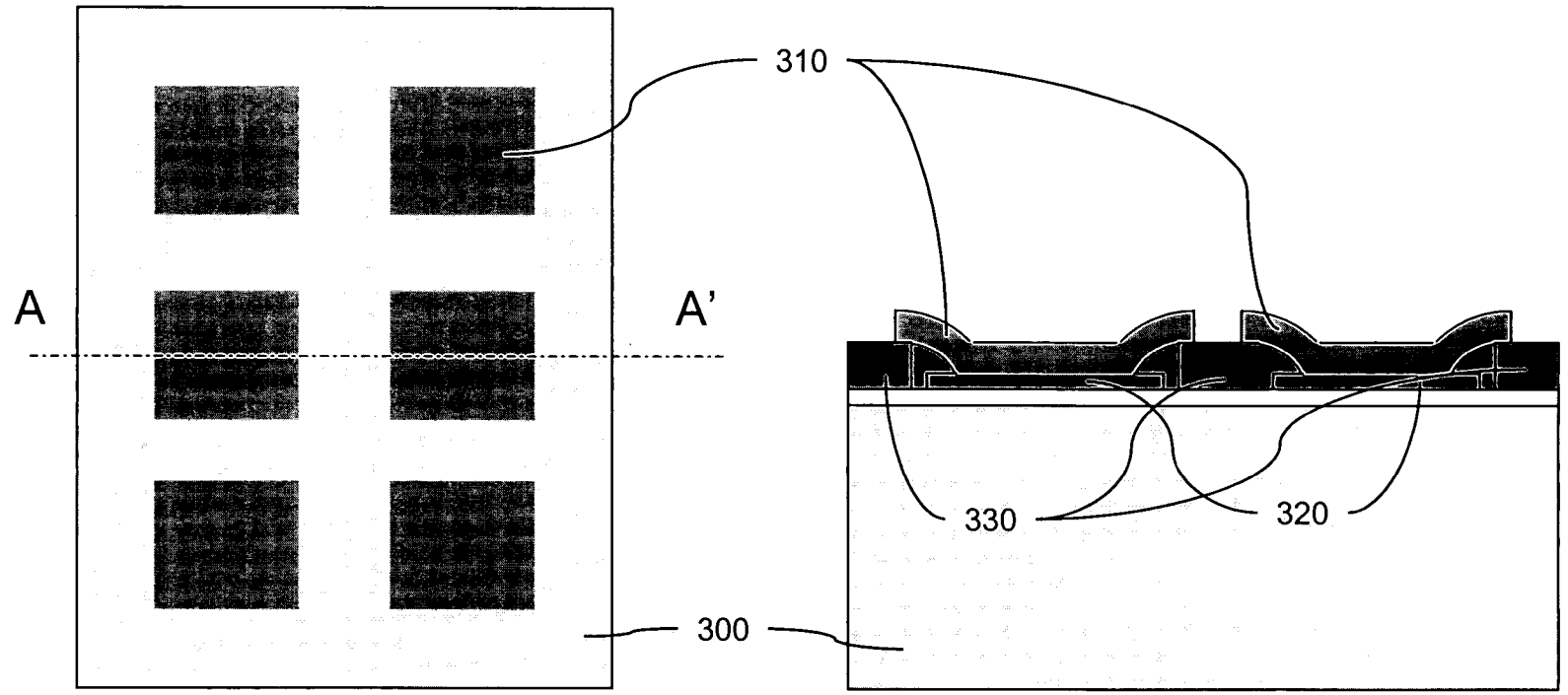
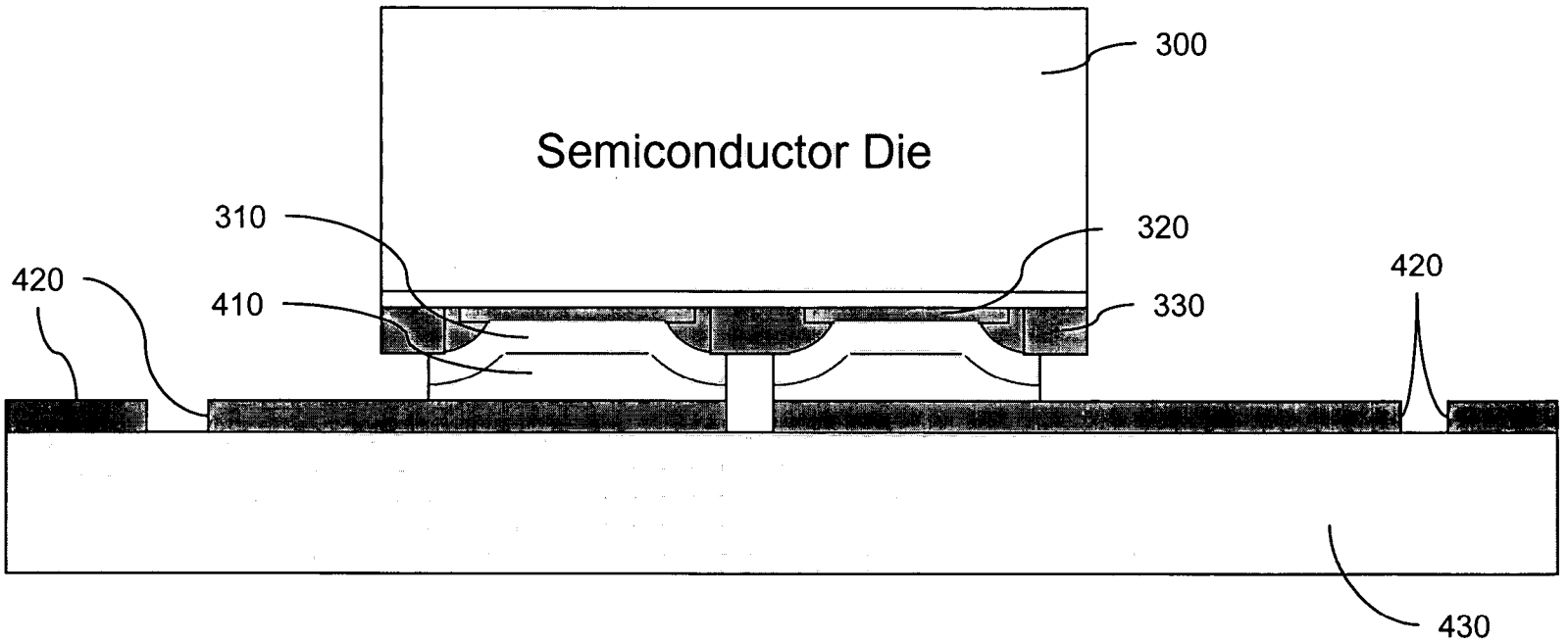


Figure 3. Die with Solderable Metal Contacts for Direct Printed Circuit Board Mounting

Semiconductor Die with Solderable Metal System Allowing Direct Surface Mounting to Printed Circuit Boards



Solderable Metal Contact Region 310

Solder

Copper Printed Circuit Board Traces 420

Printed Circuit Board 430

Figure 4. Illustration of Die with Solderable Electrical Contacts Mounted on Printed Circuit Board